VRM8.5 Multiple-Output Motherboard Power Controllers (ISL6523EVAL1, ISL6524EVAL1)

Application Note | May 2001 | AN9925

Author: Bogdan M. Duduman

Introduction

Today's high-performance desktop PC architectures demand power solutions featuring increased integration and reduced system-level costs. The Intersil ISL6523 and ISL6524 are complex controllers that integrate two and one, respectively, switching regulators, as well as two and three, respectively, linear controllers in a single package. The switching converters employ voltage-mode control architecture and high circuit performance is insured by the use of high gain-bandwidth product error amplifiers, high-accuracy references, and continuously adaptive shoot-through protection. The ICs offer a full range of protection features including overcurrent, overvoltage, as well as fault condition signaling and/or shutdown. All these combined features makes them ideal for microprocessor point-of-use power supply solutions. The ISL6523 and ISL6524 were designed to provide most of the active-state power needs of a typical Tualatin-based system. Some Coppermine-T and Celeron-based systems may also benefit from the ISL6523 or ISL6524. [1,2]

The ISL6523EVAL1 and ISL6524EVAL1 evaluation boards embody 4-output regulator solutions targeted at supplying power to the microprocessor core (1.05V - 1.825V), AGTL+ communication bus (1.2V), 4X AGP video (1.5V), and the ICH/MCH chip set core (1.8V).

Evaluation Board Setup

Important!

The evaluation boards were not designed to support a continuous V_{CORE} output current in excess of 15A for extended periods of time. When testing either board to VOUT1 output currents in excess of 15A, restrict the ON time to less than 2 minutes, followed by at least 4 minutes OFF.

To facilitate the evaluation of the ISL6523 or ISL6524 in a typical setting, both evaluation boards were designed to be powered primarily from an ATX power supply [3]. However, the boards have hook-up turret terminals that allow them to be powered from standard laboratory power supplies.

Circuit Setup

Before connecting an input supply to the board, consult the circuit schematics and familiarize yourself with the various connection options offered by either evaluation board.

➤ Set the Power-On Switch

Ensure the 'ATX ON' (**SW2**) switch is in the off position (lever pointing away from 'ATX ON' marking).

➤ Set Core Voltage SW1

SW1, by means of the on-chip D/A converter, sets the output voltage for the V_{CORE} (VOUT1) output according to the corresponding table detailed in the IC's data sheet. Consult the data sheet and set the status of the VID pins according to the core output voltage level you wish to regulate to.

➤ Hookup Guide Using Standard Bench Supplies

Connect a 5V, 16A supply to the +5VIN input, a 3.3V, 6A, supply to the +3.3VIN input, and a +12V, 100mA to the +12VIN input. Using a small jumper wire, connect the +5VIN and +5VSB inputs. Connect typical loads to all the evaluation board's outputs. Consult Table 1 for maximum loads supported by the design of the board in the configuration received; read the 'Modifications' section for information on modifying either evaluation board to meet your special needs.

➤ Hookup Guide Using a Standard ATX Supply

Connect the 20-pinATX connector to the on-board J1 mating connector. Connect typical loads to all the evaluation board's outputs. Consult Table 1 for maximum loads supported by the design of the board in the configuration received; read the 'Modifications' section for information on modifying either evaluation board to meet your special needs.

Operation

➤ Provide Power to the Board

Turn on the bench supplies. If using an ATX supply, plug it into the mains, and if it has an AC switch, turn it on. The 'ATX OFF' LED should light up, indicating the presence of 5V standby on board. Flip on the 'ATX ON' switch and the 'ATX OFF' LED should turn off. Shortly thereafter 'VTT PGOOD', 'POWER GOOD' and 'ATX PGOOD' LEDs should light up indicating power good status on all the outputs, as well as the input voltages provided by the ATX supply. If bench supplies are used, the'ATX OFF' LED will only report the status of the SW2 switch, and the 'ATX PGOOD' LED will not light up under any circumstance; the other indicators will preserve their functionality.

➤ Examine Start-Up Waveforms / Output Quality Under Varying Loads

Start-up is immediate following application of bias voltage. Using an oscilloscope or other laboratory equipment, you may study the ramp-up and/or regulation of the controlled voltages under various loading conditions. For maximum versatility, we recommend the use of a programmable electronic load.

Fault Handling

In case of a fault condition (output undervoltage on the linear outputs, or overcurrent on the switching output), the entire IC shuts down and undergoes a re-start attempt. Three consecutive fault situations on any of the outputs (single fault on VOUT4, 1.8V output) latch the chip off. Review the appropriate data sheet section for more detail.

Reference Design

General

The evaluation board is built on 2-ounce, 4-layer, printed circuit board (contact Intersil for layout plots). Most of the components specific to the evaluation board alone, which are not needed in a real computer application, are placed on the bottom side of the board. Left on top of the evaluation board are the components necessary to exemplify a typical application, as well as the user interface (input/output terminals, test points, switches, etc.).

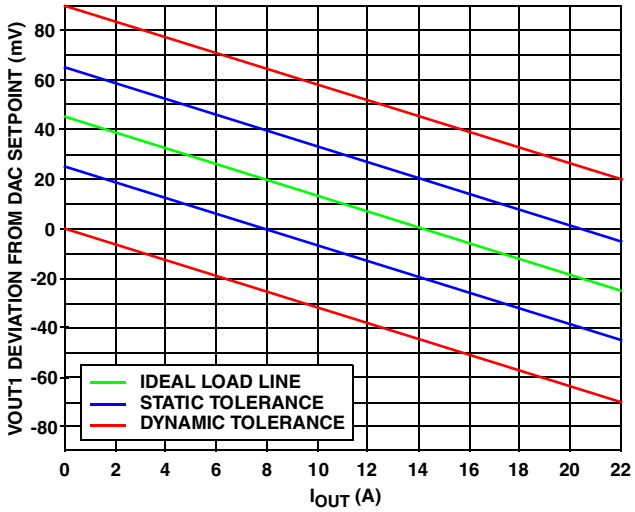


FIGURE 1. VOUT1 REGULATION ENVELOPE

VOUT1 Regulation

The core regulator (VOUT1) was designed to meet the regulation envelope detailed in Figure 1. With a DAC-set regulation point of 1.750V, the output voltage conforms to the regulation limits shown. Although the droop pictured (difference between voltage at a lesser load and voltage at a higher load) will be the same regardless of the DAC setting, the offset shown will exhibit a proportional dependence. The resistive divider sets this offset at 2.57%. For example, the ideal load line at no load and 1.600V DAC setting will actually originate at 41mV positive offset.

Design Envelope

Although an actual computer system application may have somewhat different requirements, the ISL6523EVAL1 and ISL6524EVAL1 boards were designed to meet the maximum output loading described in Table 1. Dynamic output tolerances and current ratings can be adjusted by properly selecting the components external to the ISL6523 or ISL6524.

TABLE 1. ISL6523EVAL1 MAXIMUM OUTPUT LOADING

OUTPUT VOLTAGE	I_{OUT}	dI_{OUT}/dt	TOLERANCE (STATIC/ DYNAMIC)
ISL6523EVAL1			
V_{CORE} (VOUT1)	22.0A(pk) 14.0A(avg)	20A/µs	Note 1
1.2VVTT (VOUT2)	10.0A(pk) 4.0A(avg)	1A/µs	5%/9%
1.5VAGP (VOUT3)	3.0A(pk) 1.0A(avg)	1A/µs	3%/5%
1.8VMCH (VOUT4)	3.0A(pk) 1.0A(avg)	1A/µs	3%/5%
ISL6524EVAL1			
V_{CORE} (VOUT1)	22.0A(pk) 14.0A(avg)	20A/µs	Note 1
1.2VVTT (VOUT2)	6.0A(pk) 1.0A(avg)	1A/µs	5%/9%
1.5VAGP (VOUT3)	3.0A(pk) 1.0A(avg)	1A/µs	3%/5%
1.8VMCH (VOUT4)	3.0A(pk) 1.0A(avg)	1A/µs	3%/5%

NOTE:

1. See Figure 1 for regulation tolerance details.

From a thermal performance perspective, do not operate the evaluation board for extended periods of time at output current levels exceeding the design envelope, as detailed in Table 1.

Performance

Figures 2 through 8 depict the evaluation boards' performance during typical operational situations. To simulate minimum loading conditions, unless otherwise specified, the outputs were loaded with 65Ω resistive loads. As performance is very similar amongst the two evaluation boards, some characteristics were shown for only one of them, with the implicit understanding of similarity (as appropriate).

Soft-Start Start-Up

Figure 2 shows a typical ISL6524EVAL1 start-up. For this capture, the ATX supply powering the board is turned on, at time T0. At time T1, the 1.8VMCH output starts ramping up, maintaining less than a 2V difference to the ATX3.3V output (sensed at the VAUX pin). At time T2, all input voltages reach regulation, and the 1.2VVTT output starts its ramp-up. At time T3, the 1.2VVTT output reaches VTT_PGOOD threshold and SS13 is released. Shortly after T3, the still rising SS24 brings the 1.8VMCH output in regulation. At T4, the SS13 clamp starts releasing outputs 1 and 3 (V_{CORE} and 1.5VAGP), allowing them to ramp up to their regulation levels. At time T5, all outputs controlled by the ISL6524 are within regulation limits.

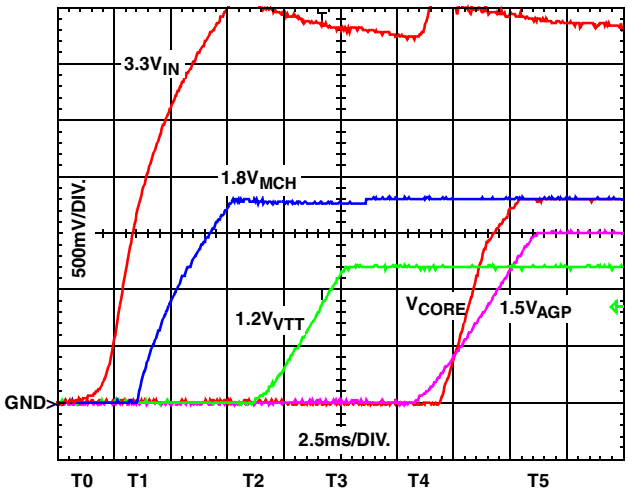


FIGURE 2. ISL6524EVAL1 START-UP

Power Good Operation

The ISL6523 and ISL6524 output two PGOOD indicators (both open-collector outputs). VTTPG is maintained high (pulled high by external pull-up resistor) as long as the 1.2VVTT output exceeds 1.08V (90%; as sensed at the VSEN pin). PGOOD is high for as long as V_{CORE} is within power good limits (+/-10%), all linears are above their undervoltage (UV) thresholds, and VTTPG is also high.

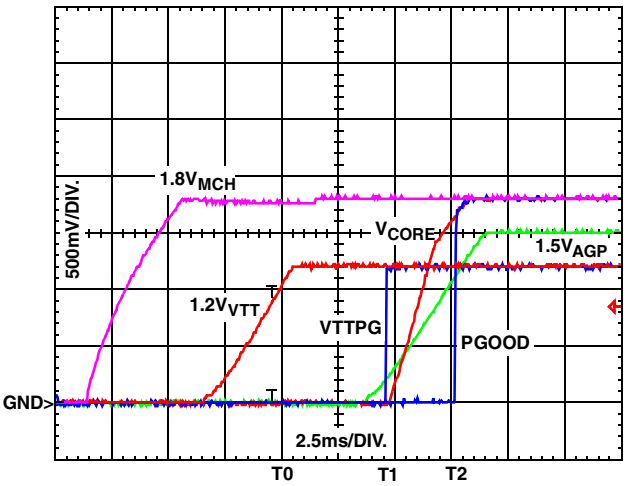


FIGURE 3. ISL6524EVAL1 POWER GOOD INDICATORS

Figure 3 details the operation of the power good functions. Following the 1.2VVTT output rising above 1.08V at time T0, VTTPG goes high simultaneously with enabling of the V_{CORE} regulator, approximately 4.5ms later. This timing delay is given by the SS13 capacitor charging under a 28µA constant current, to about 1.25V (bottom of internal oscillator ramp). To reduce the delay, while preserving the same ramping rate for the V_{CORE} output, insert a resistor (footprint provided; R18 and R22, respectively) of up to 100kΩ in series with the SS13 soft-start capacitor (100kΩ resistor should yield a 1ms delay). At time T2, all conditions met, PGOOD goes high.

Note that the two power good pins are pulled high to VTT and V_{CORE}, respectively. If TTL compatibility is desired, feel free to populate the provided spare footprints to ATX3.3V level (while de-populating the default pull-up resistors).

Transient Response

For transient response testing, the evaluation boards were subjected to the loading presented in Table 2. Each output response was recorded while the corresponding transient load was applied. The results are presented in Figures 4 and 5.

TABLE 2. TRANSIENT OUTPUT LOADING DESCRIPTION

OUTPUT	$I_{OUT(MIN)}$ (A)	$I_{OUT(MAX)}$ (A)	dI_{OUT}/dt (A/µs)	FREQUENCY (Hz)
ISL6523EVAL1				
V_{CORE} (VOUT1)	2.0	22.0	1.0	2500
1.2VVTT (VOUT2)	1.0	10.0	1.0	2000
1.5VAGP (VOUT3)	0.3	3.0	1.0	1500
1.8VMCH (VOUT4)	0.3	3.0	1.0	3000
ISL6524EVAL1				
V_{CORE} (VOUT1)	2.0	22.0	1.0	2500
1.2VVTT (VOUT2)	0.5	6.0	1.0	2000
1.5VAGP (VOUT3)	0.3	3.0	1.0	1500
1.8VMCH (VOUT4)	0.3	3.0	1.0	3000

NOTE: All transients 30% duty cycle.

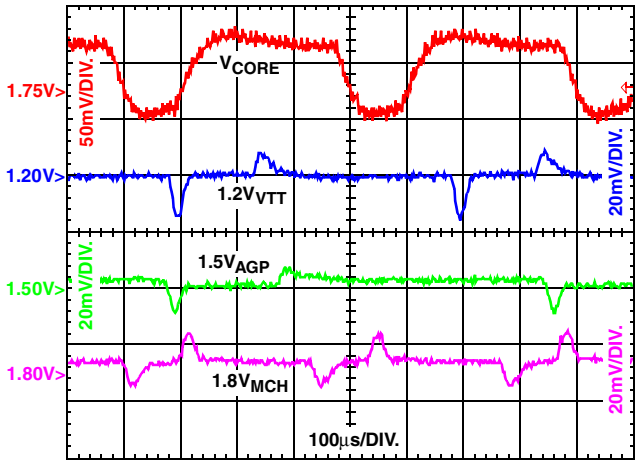


FIGURE 4. ISL6524EVAL1 OUTPUT TRANSIENT RESPONSE

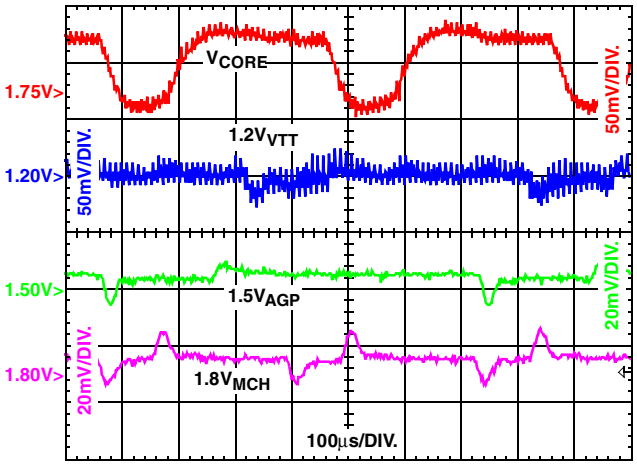


FIGURE 5. ISL6523EVAL1 OUTPUT TRANSIENT RESPONSE

Output Short-Circuit Protection

In response to an overcurrent event on the switcher's output, or an undervoltage event on any of the linear outputs, the entire chip is shut down. Figure 6 exemplifies such a scenario on VOUT1 of the ISL6524EVAL1. At time T0, an overload is applied to the core regulator output. Output current on this output increases, ultimately tripping the overcurrent (OC) protection. The fault counter is incremented and SS24 capacitor is discharged, timing a restart attempt. The restart takes place as the SS24 ramps up, and as the output voltage builds up, a second OC event is triggered at T1. The fault counter is incremented and the process repeats at time T2. At time T3 the fault counter reaches a count of three and the chip latches off. SS24 discharges down to about 1V, remaining at this level until bias voltage is removed.

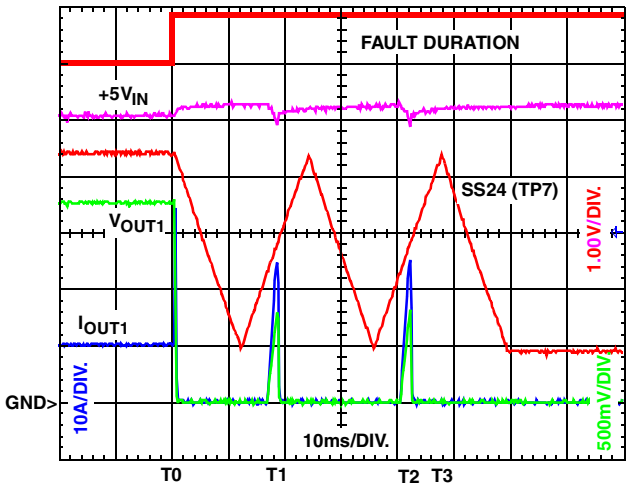


FIGURE 6A. ISL6524EVAL1 VOUT1 OVERCURRENT PROTECTION RESPONSE

The chip has two independent fault counters. Three consecutive fault events on either outputs 1 or 3, or three consecutive fault events on output 2 will set the latch. Figure 7 details an example of such a situation where the overload is removed before the counter increments to three and latches the chip off. Time T0 marks the application of the current overload. At time T1 a second fault is recorded, but the overload is removed at time T2. Second restart attempt at time T3 is successful, bringing the output in regulation and resetting the fault counter.

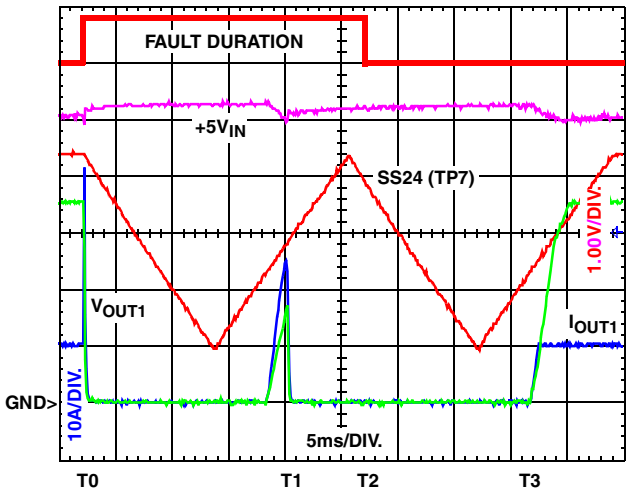


FIGURE 6B. ISL6524EVAL1 VOUT1 OVERCURRENT PROTECTION RESPONSE

ISL6524EVAL1 Switching Regulator Efficiency

Figure 7 highlights the evaluation board's conversion efficiency with only the switching section loaded (V_{CORE}). The measurement was performed at room temperature with the linear outputs open and 100 LFM of air flow.

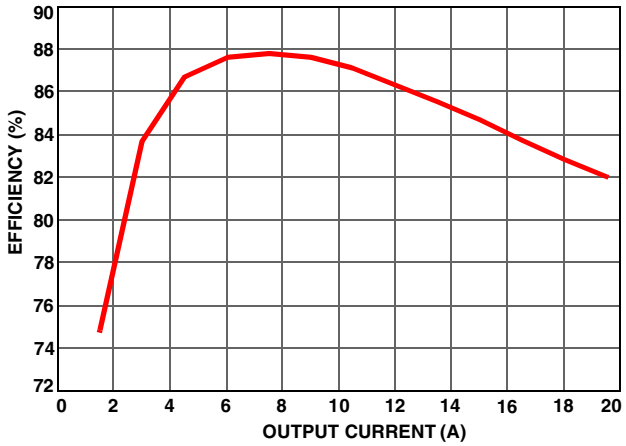


FIGURE 7. ISL6524EVAL1 SWITCHING REGULATOR MEASURED EFFICIENCY (ALL LINEAR OUTPUTS UNLOADED)

Modifications

Adjusting the Output Voltage

All linear outputs controlled by the ISL6523 and ISL6524 are adjustable by means of the resistive divider connecting the VSEN pins to their respective outputs. If adjusting the output voltage of the linear regulators, please pay attention to the recommended resistor value selection guidelines described in the data sheet. As the chips feature internal resistive dividers that set the output voltages, in order to minimize DC set-point interference with these resistors, it is recommended the parallel combination of the external resistive divider components be kept below 2kΩ to 5kΩ. Furthermore, the ISL6524 has provisions (by grounding the FIX pin) for bypassing the internal resistive dividers.

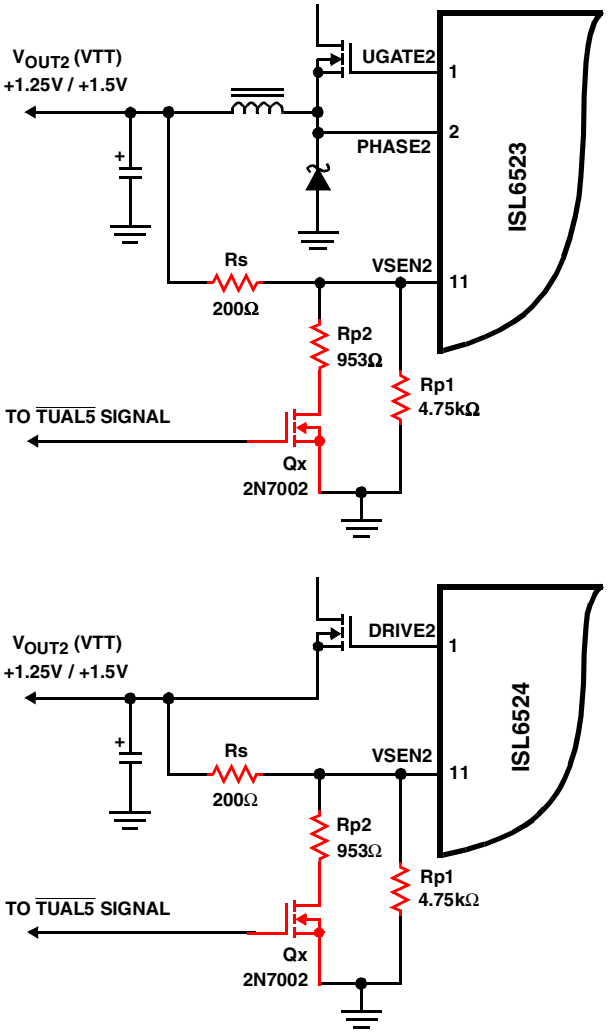


FIGURE 8. ISL6523, ISL6524 DUAL PROCESSOR GTL IMPLEMENTATION

Recommended Implementation for Dual Processor GTL VTT and Universal AGP Support

As both ICs have fixed output voltages, it is necessary to implement an external circuit that helps switch a given output between two output voltage settings. The recommended circuits for the dual processor GTL VTT and universal AGP support implementation are shown in Figures 8 and 9. As both the ISL6523 and ISL6524 were designed to regulate the voltage present at the VSEN2 pin to 1.2V, the resistive divider made out of Rs and Rp1 raise the DC regulation setting of this output to 1.25V, while Qx is off. When Qx is turned on (by means of a high $\overline{\text{TUAL5}}$ signal), Rp2 is connected in parallel to Rp1, raising the DC regulation setting of this output to 1.5V.

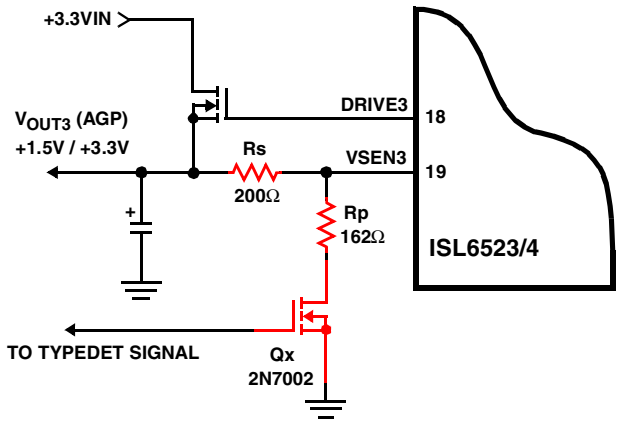


FIGURE 9. ISL6523, ISL6524 UNIVERSAL AGP SUPPORT IMPLEMENTATION

Same theory of operation applies to the circuit in Figure 9, with the exception that while Qx is off (low TYPEDET signal) the output is regulated to the internally-set 1.5V. A TYPEDET high signal turns on Qx and raises the output voltage to 3.3V. If AGP2X support is provided (3.3V output), remember that for a low voltage drop across the pass element, a low $r_{DS(ON)}$ MOSFET needs to be selected (Q4 in circuit schematics).

Important to mention is the fact that for either regulator on either IC, a sudden turn-on of Qx while the corresponding output is within regulation may trigger an undervoltage and/or overcurrent event, resulting in a chip shutdown and consequent re-start. If Qx is to be turned on while the outputs are regulating, an RC low-pass network needs be placed in series with its gate, in order to slow down its turn-on (if a pull-up is used to generate the logic high signal, then only the capacitor needs to be added). For this low-pass RC network, a time constant of about 200-300µs is recommended.

Improving Output Voltage Tolerance

The key to improving the output voltage tolerance is identifying the parameters which affect it, and then taking steps toward improving them.

AC Tolerance

High dV/dt spikes present in the output voltage waveform under highly dynamic load application (high dI/dt) are due to the ESR and the ESL of the output capacitance. These spikes coincide with the transient load's rising and falling edges, and decreasing their amplitude can be achieved by using lower ESR/ESL output capacitors (such as surface-mount tantalum capacitors), and/or the addition of more ceramic capacitors, which have inherently low ESR/ESL.

DC Tolerance

The no-load DC output voltage tolerance reduces virtually to the tolerance of the controller and that of the resistors in the DC feedback path. As the regulation tolerance of the controller is a design constraint, the only way to improve the DC regulation reduces to using precision resistors in the DC feedback path.

If output inductor based droop is employed (as shown in the default shipping configuration), the output voltage droop will also exhibit a temperature variation. As temperature will affect the DC resistance of the output inductor, the slope of the output droop will increase slightly with temperature.

VRM8.5 (Rev. 1.0) Compliance

Although the transient response of the ISL6523EVAL1 and ISL6524EVAL1 evaluation boards may prove satisfactory, to build a well designed application around any of these two controllers requires careful consideration of all the parameters involved in the output regulation. Such careful analysis of these two designs suggests that to yield a 22A VRM8.5 compliant regulator, one more capacitor is needed in parallel with the VOUT1 output (same type as already populated). Additionally, to support the increased input RMS current of a continuous 22A load, another input capacitor is also required in parallel with C1 (same type as C1).

However, compliance with this set of standards is not directly related to the use of a certain capacitor technology. Several solutions to meeting the output regulation requirements can be derived, using capacitors from various vendors, with distinctly different characteristics.

Conclusion

The ISL6523EVAL1 and ISL6524EVAL1 evaluation boards showcase highly integrated approaches to providing system power control in late Pentium 3 computer systems. Typical implementation requires minimum effort and a reduced number of external components, yet provides a full array of standard features.

References

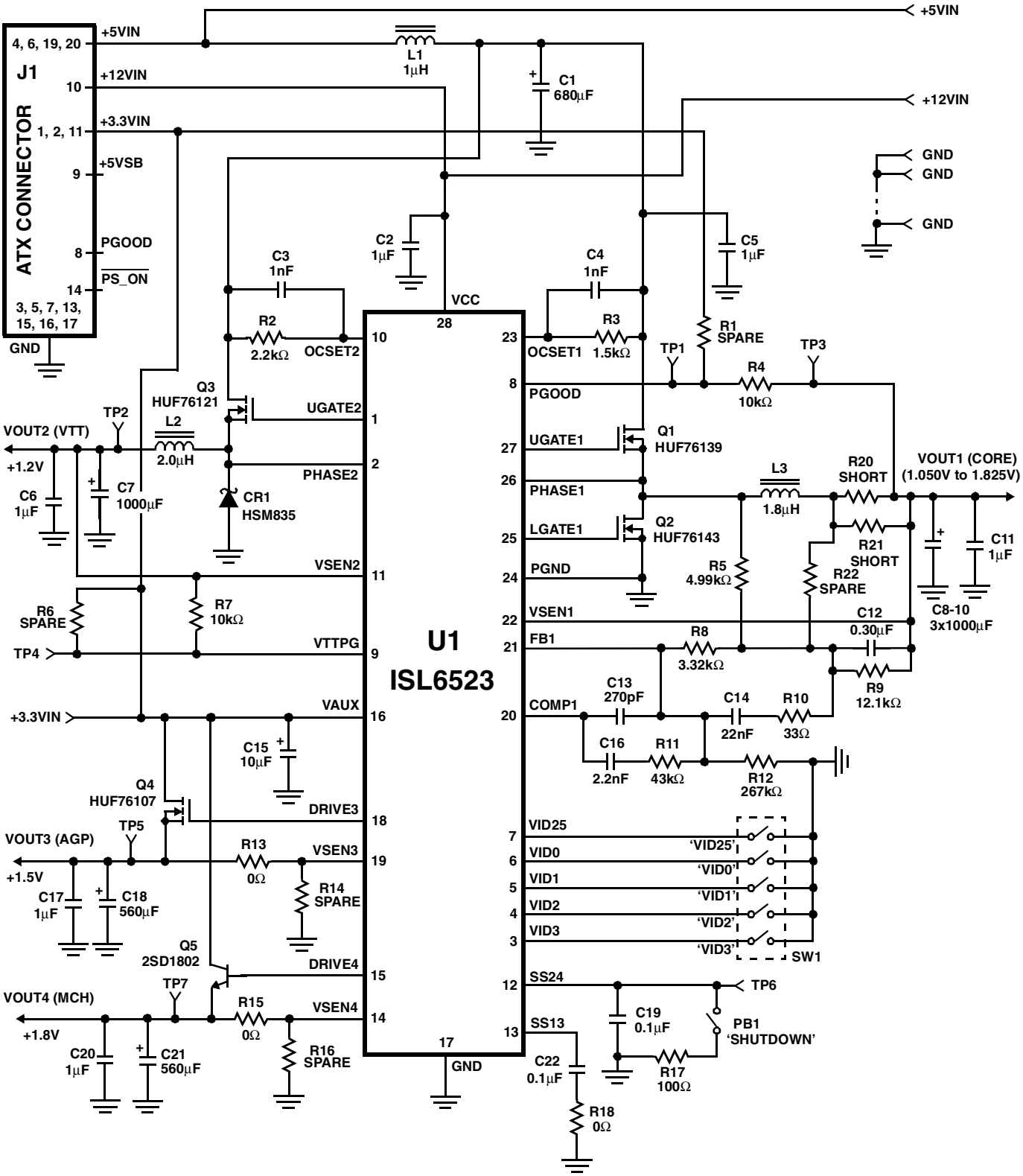
For Intersil documents available on the internet, see web site www.intersil.com/

[1] *ISL6523 Data Sheet,* Intersil Corporation, Power Management Products Division, Document No. FN9024, 2001.

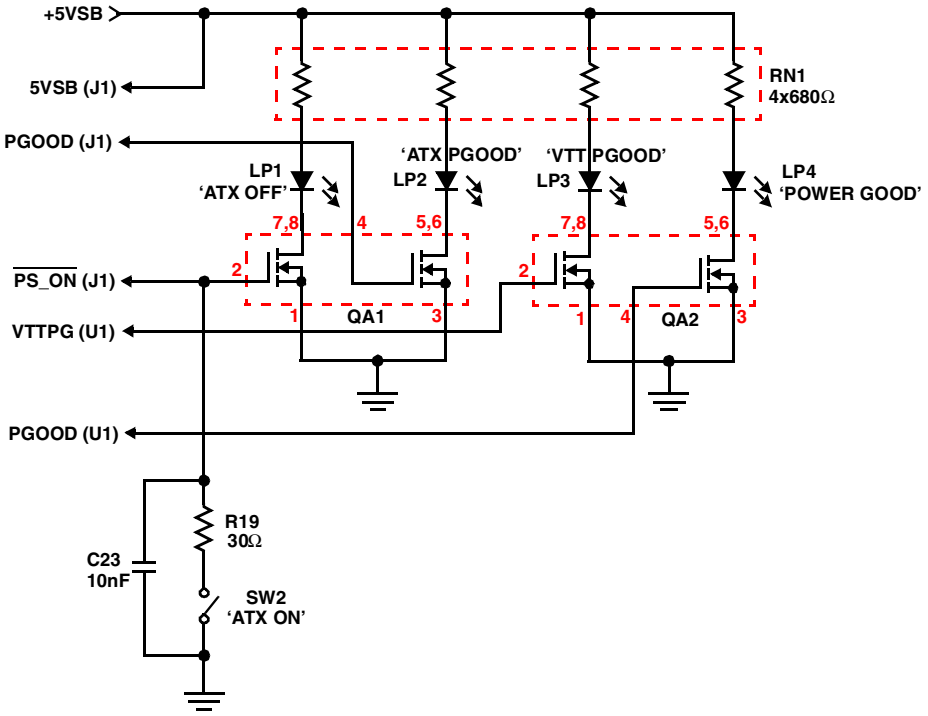
[2] *ISL6524 Data Sheet,* Intersil Corporation, Power Management Products Division, Document No. FN9015, 2001.

[3] ATX Specification, Version 2.02, October 1998, Intel Corporation (http://www.teleport.com/~atx/).

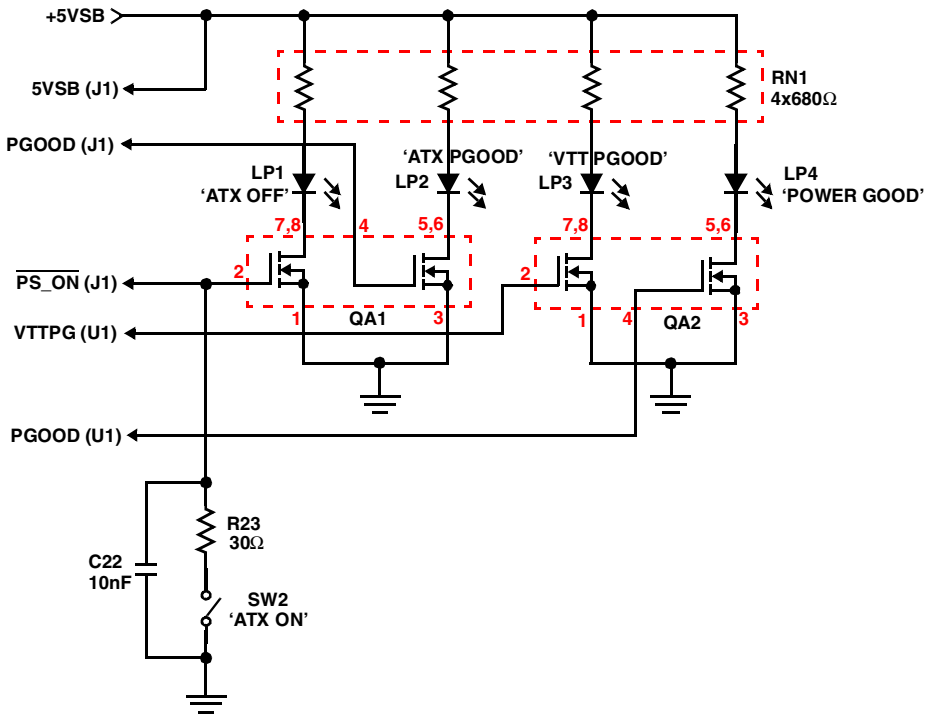
ISL6523EVAL1 Schematic



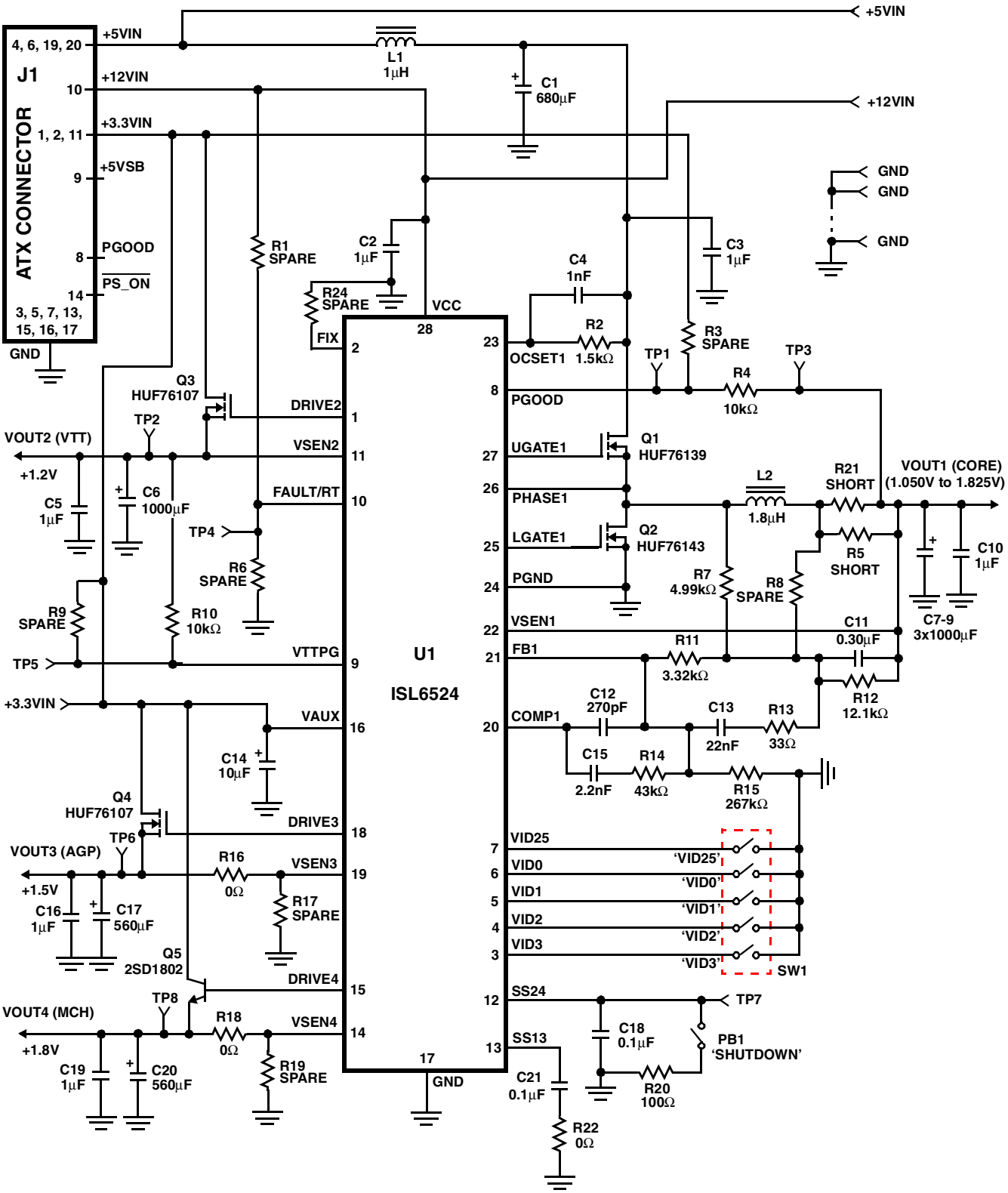
ISL6523EVAL1 Schematic (Continued)



ISL6524EVAL1 Schematic



ISL6524EVAL1 Schematic (Continued)



ISL6523EVAL1 Bill of Material s

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	CASE / FOOTPRINT	MANUF. OR VENDOR	QTY
C1	6SP680M	Oscon Capacitor, 6.3V, 680µF	10 x 10.5	Sanyo	1
C2	1206YC105KAT2A	Ceramic Capacitor, X7R, 16V, 1.0µF	1206	AVX	1
C3, 4	0603YC102KAT2A	Ceramic Capacitor, X7R, 16V, 1.0nF	0603	AVX	2
C5, 6, 11, 17, 20	1206YC105KAT2A	Ceramic Capacitor, X7R, 10V, 1.0µF	0805	AVX	5
C7-10	2SP1000M	Oscon Capacitor, 2V, 1000µF	10 x 10.5	Sanyo	4
C12	0805ZC304KAT2A	Ceramic Capacitor, X7R, 10V, 0.30µF	0805	AVX	1
C13	06033C271KAT2A	Ceramic Capacitor, X7R, 25V, 270pF	0603	AVX	1
C14	06033C223KAT2A	Ceramic Capacitor, X7R, 25V, 22nF	0603	AVX	1
C15	TAJB106M006R	Tantalum Capacitor, 6.3V, 10µF	3.0 x 4.0	AVX	1
C16	06033C222KAT2A	Ceramic Capacitor, X7R, 25V, 2.2nF	0603	Any	1
C18, C21	4SP560M	Oscon Capacitor, 4V, 560µF	8 x 10.5	Sanyo	2
C19, C22	0603ZC104KAT2A	Ceramic Capacitor, X7R, 10V, 0.1µF	0603	AVX	2
C23	0603YC103KAT2A	Ceramic Capacitor, X7R, 16V, 10nF	0603	AVX	1
CR1	HSM835J	Schottky Diode, 35V, 8A	DO-214AB	Microsemi	1
J1	39-29-9203	20-pin Mini-Fit, Jr.™ Header Connector		Molex	1
L1	1.0µH Inductor	6 Turns of 16AWG onT44-52 Core	8 x 15	Any	1
L2	2.0µH Inductor	8 Turns of 16AWG on T50-52 Core	8 x 17	Any	1
L3	1.8µH Inductor	6 Turns of 16-18AWG on T68-52 Core	10 x 21	Any	1
LP1-4	L63111CT-ND	Miniature LED, Through-Board Indicator		Digikey	4
Q1	HUF76139S3S	UltraFET™ MOSFET, 30V, 7.5mΩ	TO-263AB	Intersil	1
Q2	HUF76143S3S	UltraFET™ MOSFET, 30V, 5.5mΩ	TO-263AB	Intersil	1
Q3	HUF76121D3S	UltraFET™ MOSFET, 30V, 23mΩ	TO-252AA	Intersil	1
Q4	HUF76107D3S	UltraFET™ MOSFET, 30V, 52mΩ	TO-252AA	Intersil	1
Q5	2SD1802	NPN Bipolar, 50V, 3A	TO-252AA	Sanyo	1
QA1, 2	ZXMD63N02X	Small-Signal Dual MOSFET, 20V, 0.2Ω	MSOP-8	Zetex	2
PB1	P8007S-ND	Push-Button, Miniature		Digikey	1
R2	2.2kΩ	Resistor, 5%, 0.1W	0603	Any	1
R3	1.5kΩ	Resistor, 5%, 0.1W	0603	Any	1
R4, 7	10kΩ	Resistor, 5%, 0.1W	0603	Any	2
R5	4.99kΩ	Resistor, 1%, 0.1W	0603	Any	1
R8	3.32kΩ	Resistor, 1%, 0.1W	0603	Any	1
R9	12.1kΩ	Resistor, 1%, 0.1W	0603	Any	1
R10	33Ω	Resistor, 5%, 0.1W	0603	Any	1
R11	43kΩ	Resistor, 5%, 0.1W	0603	Any	1
R12	267kΩ	Resistor, 1%, 0.1W	0603	Any	1
R13, 15, 18	0Ω	Shorting Resistor	0603	Any	3
R17	100Ω	Resistor, 5%, 0.1W	0603	Any	1
R19	30Ω	Resistor, 5%, 0.1W	0603	Any	1
R1, 6, 14, 16	Spare		0603		
R20, 21	Spare		2512		
R22	Spare		0603		
RN1	Y9681CT-ND	4-Resistor Network, 680Ω, 5%, 0.1W	3.2 x 1.6	Digikey	1
SW1	CKN3057-ND	Miniature Dip Slide Switch, 5-Pole		Digikey	1
SW2	GT12MSCKE	Miniature Switch, Single Pole, Single Throw		C&K	1
TP2, 3, 5, 7	1314353-00	Test Point, Scope Probe		Tektronics	4
TP1, 4, 6	SPCJ-123-01	Test Point		Jolo	3
U1	ISL6523CB	Dual Switcher and Dual Linear Controller	SOIC-28	Intersil	1
+5VSB, +5VIN, +3.3VIN, +12VIN, $+V_{OUT1}$, $+V_{OUT2}$, $+V_{OUT3}$, $+V_{OUT4}$, GND	1514-2	Terminal Post		Keystone	16

ISL6524EVAL1 Bill of Material s

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	CASE / FOOTPRINT	MANUF. OR VENDOR	QTY
C1	6SP680M	Oscon Capacitor, 6.3V, 680µF	10 x 10.5	Sanyo	1
C2	1206YC105KAT2A	Ceramic Capacitor, X7R, 16V, 1.0µF	1206	AVX	1
C4	0603YC102KAT2A	Ceramic Capacitor, X7R, 16V, 1.0nF	0603	AVX	2
C3, 5, 10, 16, 19	1206YC105KAT2A	Ceramic Capacitor, X7R, 10V, 1.0µF	0805	AVX	5
C6-9	2SP1000M	Oscon Capacitor, 2V, 1000µF	10 x 10.5	Sanyo	4
C11	0805ZC304KAT2A	Ceramic Capacitor, X7R, 10V, 0.30µF	0805	AVX	1
C12	06033C271KAT2A	Ceramic Capacitor, X7R, 25V, 270pF	0603	AVX	1
C13	06033C223KAT2A	Ceramic Capacitor, X7R, 25V, 22nF	0603	AVX	1
C14	TAJB106M006R	Tantalum Capacitor, 6.3V, 10µF	3.0 x 4.0	AVX	1
C15	06033C222KAT2A	Ceramic Capacitor, X7R, 25V, 2.2nF	0603	Any	1
C17, C20	4SP560M	Oscon Capacitor, 4V, 560µF	8 x 10.5	Sanyo	2
C18, C21	0603ZC104KAT2A	Ceramic Capacitor, X7R, 10V, 0.1µF	0603	AVX	2
C22	0603YC103KAT2A	Ceramic Capacitor, X7R, 16V, 10nF	0603	AVX	1
J1	39-29-9203	20-pin Mini-Fit, Jr.™ Header Connector		Molex	1
L1	1.0µH Inductor	6 Turns of 16AWG on T44-52 Core	8 x 15	Any	1
L2	1.8µH Inductor	6 Turns of 16-18AWG on T68-52 Core	10 x 21	Any	1
LP1-4	L63111CT-ND	Miniature LED, Through-Board Indicator		Digikey	4
Q1	HUF76139S3S	UltraFET™ MOSFET, 30V, 7.5mΩ	TO-263AB	Intersil	1
Q2	HUF76143S3S	UltraFET™ MOSFET, 30V, 5.5mΩ	TO-263AB	Intersil	1
Q3, Q4	HUF76107D3S	UltraFET™ MOSFET, 30V, 52mΩ	TO-252AA	Intersil	2
Q5	2SD1802	NPN Bipolar, 50V, 3A	TO-252AA	Sanyo	1
QA1, QA2	ZXMD63N02X	Small-Signal Dual MOSFET, 20V, 0.2Ω	MSOP-8	Zetex	2
PB1	P8007S-ND	Push-Button, Miniature		Digikey	1
R2	1.5kΩ	Resistor, 5%, 0.1W	0603	Any	1
R7	4.99kΩ	Resistor, 1%, 0.1W	0603	Any	1
R4, R10	10kΩ	Resistor, 5%, 0.1W	0603	Any	2
R11	3.32kΩ	Resistor, 1%, 0.1W	0603	Any	1
R12	12.1kΩ	Resistor, 1%, 0.1W	0603	Any	1
R13	33Ω	Resistor, 5%, 0.1W	0603	Any	1
R14	43kΩ	Resistor, 5%, 0.1W	0603	Any	1
R15	267kΩ	Resistor, 1%, 0.1W	0603	Any	1
R16, R18, R22	0Ω	Shorting Resistor	0603	Any	3
R20	100Ω	Resistor, 5%, 0.1W	0603	Any	1
R23	30Ω	Resistor, 5%, 0.1W	0603	Any	1
R1, R3, R6, R8, R9, R17, R19, R24	Spare		0603		
R5, R21	Spare		2512		
RN1	Y9681CT-ND	4-Resistor Network, 680Ω, 5%, 0.1W	3.2 x 1.6	Digikey	1
SW1	CKN3057-ND	Miniature Dip Slide Switch, 5-Pole		Digikey	1
SW2	GT12MSCKE	Miniature Switch, Single Pole, Single Throw		C&K	1
TP2, 3, 6, 8	1314353-00	Test Point, Scope Probe		Tektronics	4
TP1, 4, 5, 7	SPCJ-123-01	Test Point		Jolo	4
U1	ISL6524CB	Dual Switcher and Dual Linear Controller	SOIC-28	Intersil	1
+5VSB, +5VIN, +3.3VIN, +12VIN, $+V_{OUT1}$, $+V_{OUT2}$, $+V_{OUT3}$, $+V_{OUT4}$, GND	1514-2	Terminal Post		Keystone	16

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
2401 Palm Bay Rd., Mail Stop 53-204
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil Ltd.
8F-2, 96, Sec. 1, Chien-kuo North,
Taipei, Taiwan 104
Republic of China
TEL: 886-2-2515-8508
FAX: 886-2-2515-8369